ISTFA 2023: Proceedings of the 49th International
Symposium for Testing and Failure Analysis Conference
November 12—16, 2023, Phoenix, Arizona, USA
https://doi.org/10.31339/asm.cp.istfa2023p0141

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Incorporating Time-Domain Reflectometry in Chip-Level Failure Analysis Workflow: Case Studies

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Abstract— Non-destructive electrical fault isolation (FI) techniques such as emission- and laser-based techniques have been utilized widely for chip-level failure analysis (FA). However, these techniques by themselves can sometimes be inadequate for certain failure modes. In this paper, we present six FA case studies using Time-Domain Reflectometry (Electro-optical terahertz pulse reflectometry) in combination with the traditional FI techniques.

Keywords—, TDR, EOTPR, LIT, Input/Output Leakage, Frequency Sensitive I/O Failures

I. Introduction

Failure Analysis (FA) of semiconductor integrated circuits (ICs) encounters ever-increasing challenges as the advancement of semiconductor process and packaging technologies continues. Non-destructive electrical failure isolation (FI) techniques such as emission-based and laser-based techniques have been utilized widely in the semiconductor industry. However, these techniques by themselves are sometimes inadequate to diagnose certain failure modes, particularly in the area where marginalities of process technologies and of packaging technologies overlap.

In recent years, Surface Mount Technology (SMT) industry has adopted Lock-in Thermography (LIT) to localize defects such Power Shorts, IO resistive short or leakage, even though its initial aim is hotspot detection through the backside of silicon die, especially for stacked die [1,2]. Time-domain reflectometry (TDR), on the other hand, has been only used by IC packaging industry to detect discontinuity (mostly opens) in the signal path, mainly due to the lack of resolution into silicon die. To address the challenges in advanced packaging such as multi-chip modules and 2.5D CoWoS, just to name a few, Electro-optical terahertz pulse reflectometry (EOTPR) has demonstrated its capability to improve resolution [3-7].

FA engineers investigating chip-level failures always keep an open mind and consider all possibilities, as the failure could be on the silicon die or on the package. Therefore, it's only fitting that we exhaust all non-destructive (and minimally invasive) FA efforts before subjecting the failed silicon chip to destructive analysis. In this paper, we present six case studies of various failure modes; and during the course of these failure analyses, we demonstrate that EOTPR can be a valuable technique in the workflow for chip-level FA.

II. Case studies

The FI techniques at our disposal include Photon Emission Microscopy (PEM) Analysis, Curve Tracer Analysis (IVCT), EOTPR, LIT, C-mode Scanning Acoustic Microscopy (CSAM) Analysis, 2D/3D Xray Analysis, and destructive Physical Failure Analysis (PFA).

A. *Failure Analysis of uHAST Package Qual VOH/VOL Failures*

Techniques used: PEM, Curve Trace on VOH/VOL ATE setup, DC IVCT, EOTPR, LIT, and PFA

B. *Failure Analysis of HTS Pre-Qual Marginal VIL/VOL Failure*

Techniques used: EOTPR, CSAM, and PEM

C. *Failure Analysis of Field Frequency Sensitive Failure*

Techniques used: EOTPR

D. *Failure Analysis of Package Qual OPEN Failure*

Techniques used: EOTPR, Curve Trace, Xray, CSAM, LIT, and PFA

E. *Failure Analysis of Package Qual OPEN Failure*

Techniques used: EOTPR, CSAM, Xray, and PFA

F. *Failure Analysis of Customer Return OPEN Failure*

Techniques used: Curve Trace, EOTPR, LIT, and PFA

FA Technique	PEM	Power-on IVCT	DC IVCT	EOTPR	LIT	X-ray	CSAM	PFA
Case A	x	x	x	x	x			x
Case B	x			x			x	
Case C				x				
Case D			x	x	x	x	x	x
Case E				x		x	x	x
Case F			x	x	x			x

Figure 1. Fault Isolation techniques employed for each FA case

Case A. Failure Analysis of Package Qual VOH/VOL Failures

A unit with a single pin (FBA_CMD20) failing VOH/VOL tests on ATE (Automated Test Equipment) was submitted for analysis. Further curve trace characterization of the DUT (Device Under Test) in the ATE power-up mode reported that the pin was stuck at mid-level at VOH/VOL mode. Photon emission microscopy (PEM) analysis was performed on the failing pin (FBA_CMD20), with the pin being conditioned in the failure mode on ATE with additional DC biasing via a curve tracer. Several anomalous emission sites were revealed, which

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were later identified to be tied to local ground. Discussion with Design Engineering (DE) suspected a likely grounding issue as the cause of failure.

During the same PEM acquisition, we observed that the ESD and CDM diodes of a neighboring pin (FBA_CMD15) were also emitting excessive photons. This pin (FBA_CMD15) was not reported to fail, nor was it set up and biased in the test mode. But the observation provided another data point to support the theory of a likely grounding issue (Figures 2 and 3).

Another unit with similar failure mode and PEM signature was previously submitted for destructive PFA to focus on the photon-emitting transistors. However, no anomalies were revealed.

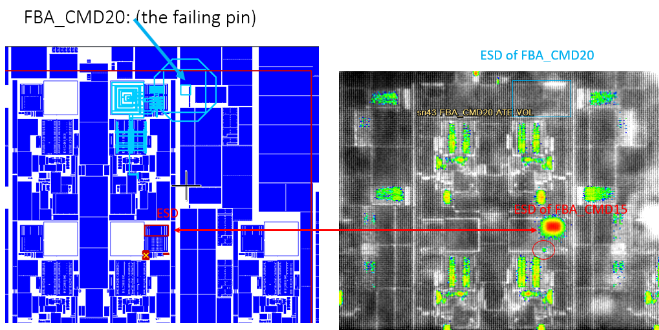

Figure 2. PEM of FBA_CMD20 in failure mode

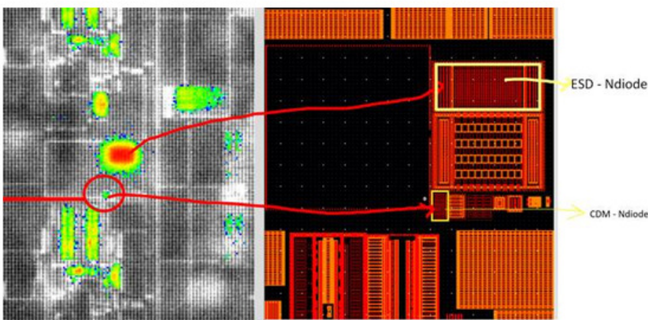

Figure 3. Review with Design on transistor functionality

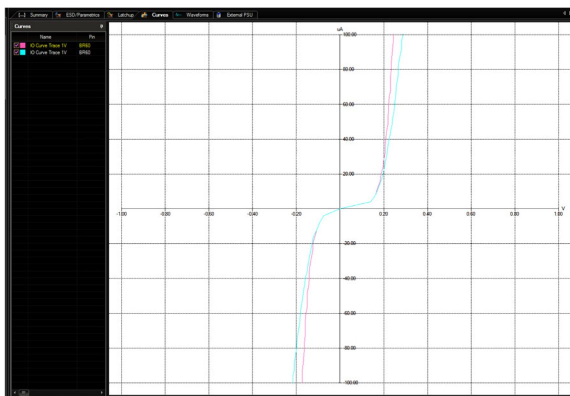

Figure 4. IV curves of failing (blue) and passing (pink) I/O pins

To further our investigation, we started to request IV characterization of I/O pins to be done before submission to the FA lab. A slight shift in IV curve was observed (Figure 4), which usually meant a discontinuity in the path of the IO to ground (GND).

To understand how a slight shift in IV curve would have caused the VOH/VOL to be stuck on ATE, we started with two theories: 1) an internal cell in the signal path was blown, or 2) the integrity of the bump-RDL interface was compromised. For Theory #1, we used the ELITE system by Thermo Fisher Scientific (Figure 5); for Theory #2, we used the EOTPR-4000 system by TeraView (Figure 6).

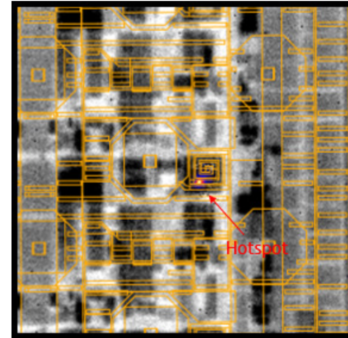

Figure 5. Backside Lock-in Thermography (LIT) showing a hotspot on the frontside of silicon

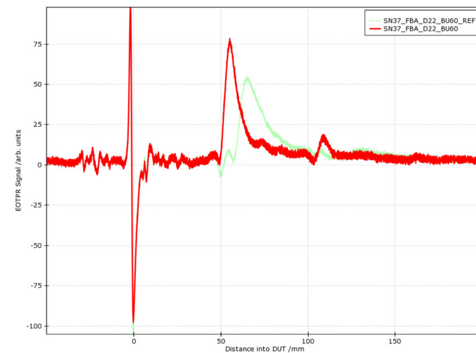

Figure 6. EOTPR waveforms of failing pin vs reference indicating the discontinuity occurred before entering the internal circuity

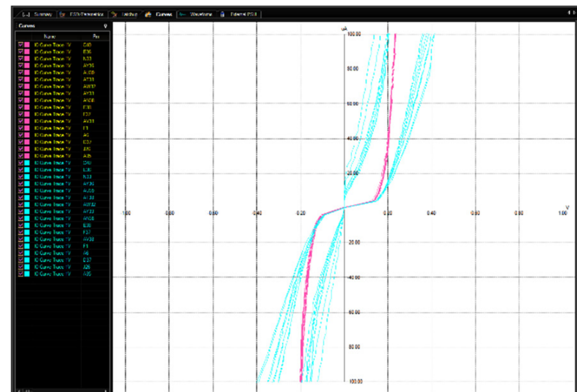

Figure 7. DC IV curves ranging from low-ohmic shorts through the origin to high-resistive curves after turn-on.

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Subsequent destructive PFA by front-side parallel lapping and optical inspection of the hotspot area revealed electrical overstress (EOS) damage at the RDL and/or top metal layer.

For the remaining qual failures of similar failure modes, we started by acquiring and reviewing DC IV curves of pins that were failing on ATE. Figure 7 plots the DC IVCTs of all ATE-reported failing pins on one DUT; the IV curves ranged from low-ohmic shorts through the origin to high-resistive curves post turned-on, with some pins passing on IVCT.

LIT and EOTPR were performed on select pins and similar signature in thermal behavior and EOTPR waveforms were observed. Combining these observations with PFA results, we are confident that LIT can be used to detect certain types of high impedance failures that are in a series or parallel connection in the signal path [8]), and that EOTPR can be used to detect certain Short or leakage failures.

CASE B. FAILURE ANALYSIS OF PRE-QUAL MARGINAL VIL/VOL FAILURE

A GPU with a single pin marginally failing VIL/VOL was submitted for EFA. Based on what we learned from Case A, we set up EOTPR to capture subtle abnormalities, even though no curve trace anomalies were reported. While performing EOTPR, the principal investigator identified three GND pins surrounding the pin of interest, and subsequent EOTPR acquisition on the failing pin against three GND pins revealed slight shifts in the waveforms, indicative of a grounding issue.

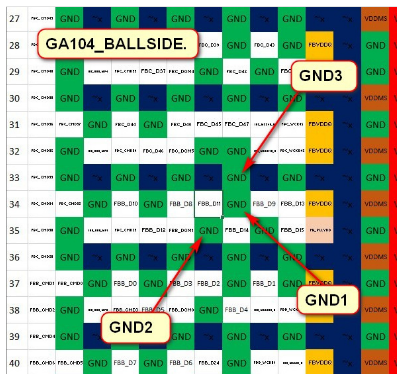

Figure 8. Ballside BGA map showing the failing pin with three GND pins

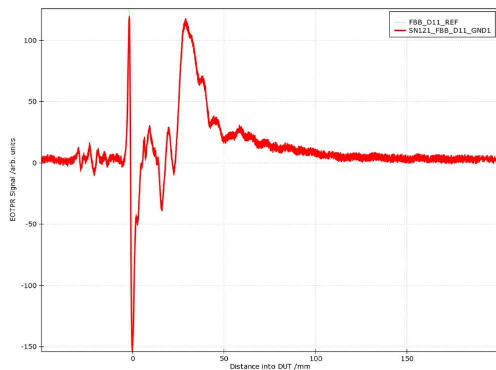

Figure 9(a). GND 1 - normal

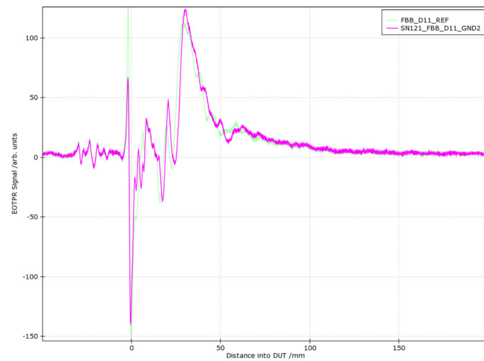

Figure 9(b). GND 2 – slight shift

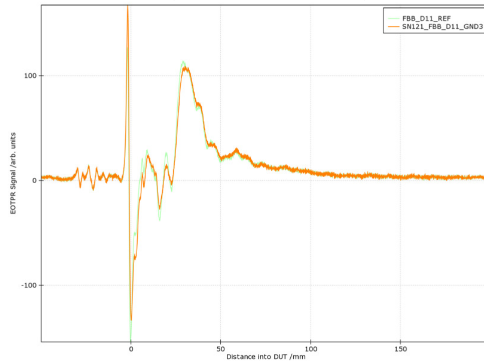

Figure 9(c). GND 3 – slight shift

Figure 9. EOTPR waveforms of the failing pin vs three GND pins

The cause of failure was consistent with CSAM observation, which showed a "white bump" on one of the GNDs. PEM in the ATE failing mode also showed a much brighter photon emission site when compared with a reference unit, indicative of higher leakage at the emitting cell.

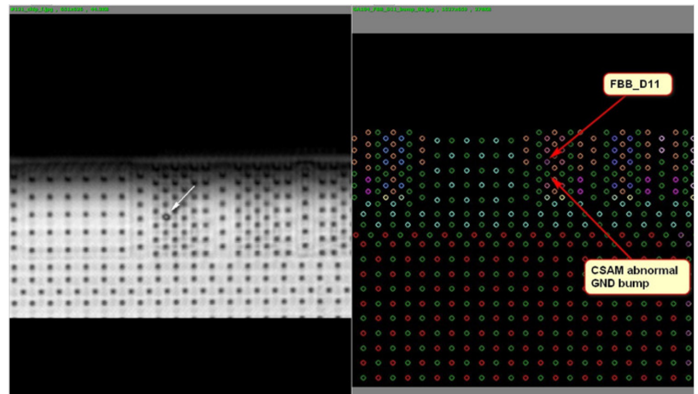

Figure 10. CSAM image showing *white bump* on GND next to the failing signal pin

CASE C. FAILURE ANALYSIS OF FIELD RETURN OF FREQUENCY SENSITIVE IO FAILURE

A couple of GPUs failing for "Bad Display" were returned for FA. These units passed on ATE across all voltages, frequencies, and temperatures, and failed intermittently on System Level Testing (SLT). The failures appeared to be sensitive to frequency, but they were so intermittent that a

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pass/fail criterium could not be established. Initial examination of the manufacturing and assembly lot data did not reveal out-of-spec parameters.

Based on the positive experience we gained with EOTPR, we decided to use EOTPR to characterize the failures. The EOTPR waveforms did not show difference in the optical delay/distance; however, the principal investigator did notice a difference in the relative "amplitude" in the package substrate, where the reference unit showed less impedance.

Discussion with Packaging Engineering revealed that, although the passing and failing units would come from the same wafer lots and same assembly sites, the substrate material of the failing units was different from that of the passing units. EOTPR acquisition confirmed the subtle difference in substrate material to be the cause of this frequency-sensitive failure.

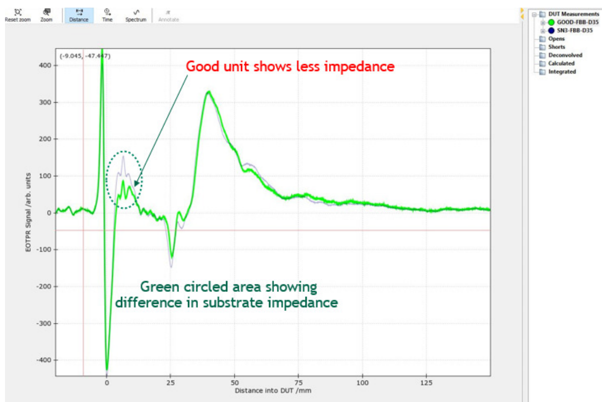

Figure 11. EOTPR waveform showing the good unit exhibiting less impedance in the package substrate

Case D. Failure Analysis of Package Qual Open Failures

Several GPUs failing continuity OPEN on ATE were submitted for FA. An EOTPR binary search using the bare substrate as the separation point allows us to quickly eliminate the package and to focus on the interfaces of Bump/RDL/Die.

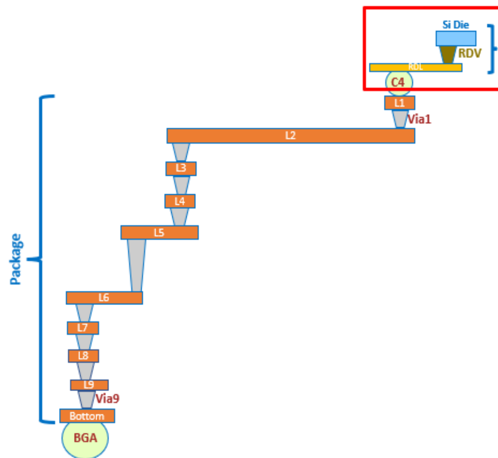

Figure 12. Cross-sectional view of traces and layers of failing signal. OPEN was isolated to the red-highlighted area.

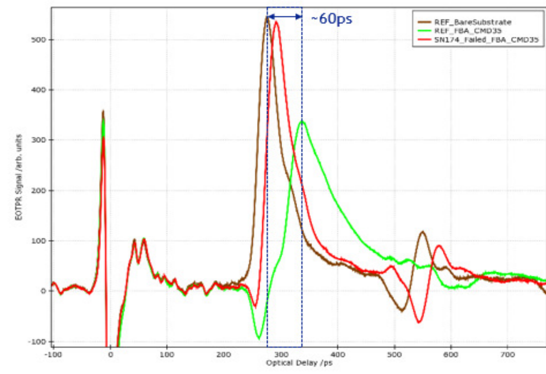

Figure 13(a). FB Pins: Delta ~60ps

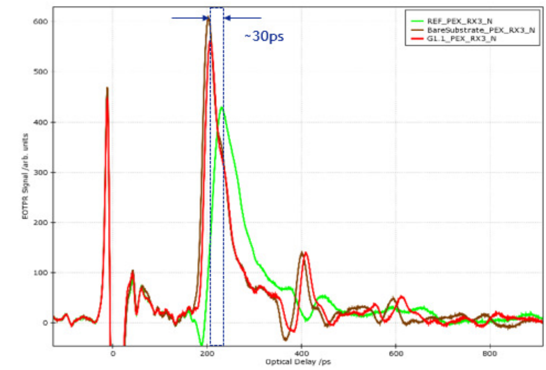

Figure 13(b). PEX Pins: Delta ~30ps

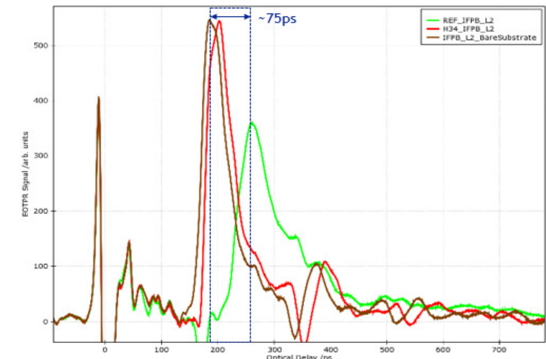

Figure 13(c). IFP Pins: Delta ~75ps

Figure 13. EOTPR waveforms of bare substrate (brown), fail (red), and reference (green). Deltas of optical delays between bare substrate and reference are 60ps (a), 30ps (b), and 75ps (c) for three different types of IO pins.

Product	Signal Name	Optical Delay (ps)	Optical Delay (ps)	Delta Optical Delay (ps)
		Pin_REF-KnownGoodDie	Pin_Substrate-Bare-CuPillar	Pin_(KGD-CuP)
GPU10x	FB_1	338.6	276.3	62.3
GPU10x	FB_2	328.3	268.4	59.9
GPU10x	FB_3	322.3	261	61.3
GPU10x	FB_4	305.8	244.5	61.3
GPU10x	PEX_1	234.1	204	30.1
GPU10x	PEX_2	236	205	31
GPU10x	IFP_1	296.5	220	76.5
GPU10x	IFP_2	346	271	75

Figure 14. Deltas of optical delays between bare substrate (CuPillar) and reference (Known Good Die) for three different types of IO pins.

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Conventional transmission line modeling and EOTPR simulation usually assumes that the laser pulse signal would quickly drop off once it enters the silicon die. Therefore, it was expected that the delta in optical delays between the bare substrate and the reference unit (Known Good Die) should be roughly the same for devices of the same product family (with same design and process technology). However, the measured deltas appear to vary significantly for different types of IO pins: 60ps, 30ps, and 75ps, for the three types of IOs that we analyzed (Figures 13 and 14.) This indicates that the capacitive coupling effect of silicon die can have a stronger dependency on the IO design and layout density than what was previously assumed. For future simulation and modeling to be accurate, we may have to take this effect into consideration.

CASE E. FAILURE ANALYSIS OF PACKAGE QUAL OPEN FAILURES

One CPU failing continuity OPEN on ATE was submitted for FA. We again used EOTPR binary search using the bare substrate as the separation point which allows us to quickly determine how and where to direct our analysis efforts.

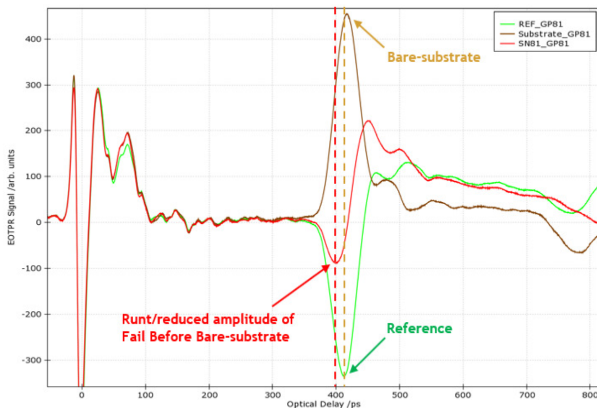

Figure 15. EOTPR waveforms of bare substrate (brown), fail (red), and reference (green).

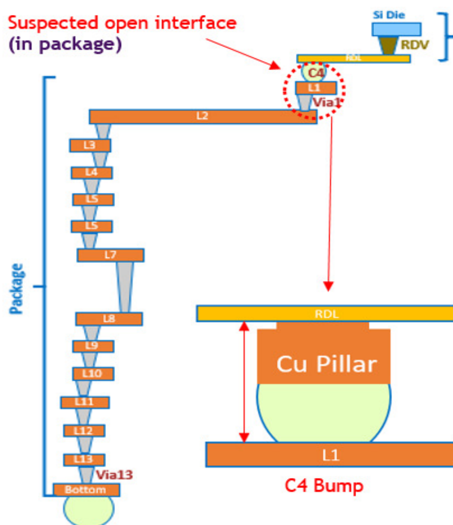

Figure 16. Cross-sectional view of traces and layers of failing signal. OPEN was isolated to the red-highlighted area.

EOTPR quickly revealed a runt (reduced amplitude) "valley" with the optical delay before that of the bare substrate (Figure 15.) Consultation with the cross-sectional view of traces and layers suggests the OPEN in the interface of end-of-trace in package and the C4 bump (Figure 16.)

We continued the non-destructive analysis efforts to this interface: high resolution 3D Xray scan identified an anomalous "dashed-line" across the target bump in comparison with its neighboring bumps that are not failing (Figure 17.) Crack at the target bump was later confirmed by FIB cross-section when PFA resources became available.

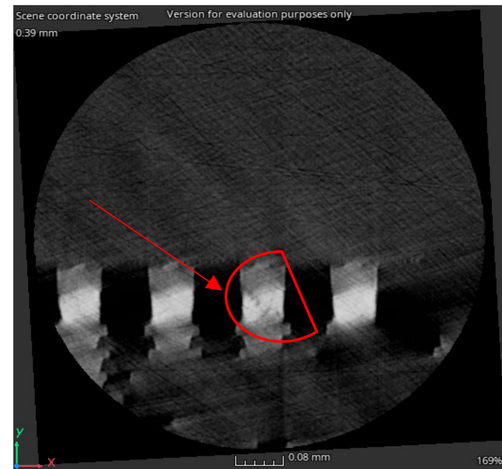

Figure 17. 3D Xray showing crack in the target bump.

CASE F. FAILURE ANALYSIS OF CUSTOMER RETURN OPEN FAILURES

Product Quality Engineering (PQE) submitted one customer return GPU for FA. The unit failed continuity OPEN at the board-level SLT. Because these IO pins are not designed to allow direct access for field applications, they are not tested directly on ATE. PQE verified the OPEN failure on curve tracer.

Since this is a CoWoS GPU, our EOTPR binary search requires waveform acquisitions of the bare substrate and of the silicon interposer to narrow down the location of the fault.

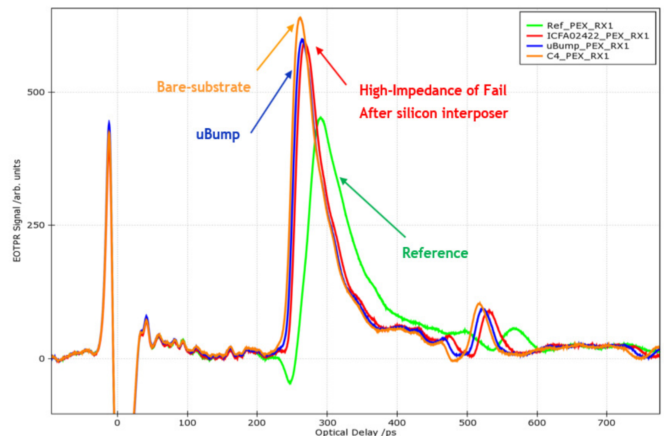

Figure 18(a). Full waveform

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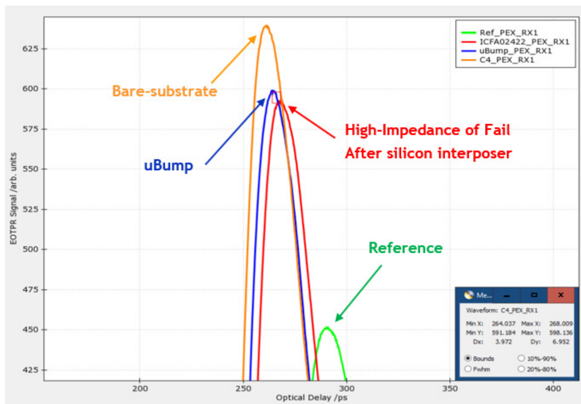

Figure 18(b). Zoom-in at the peaks

Figure 18. EOTPR waveforms of bare substrate (brown), silicon interposer (uBump, blue), fail (red), and reference (green).

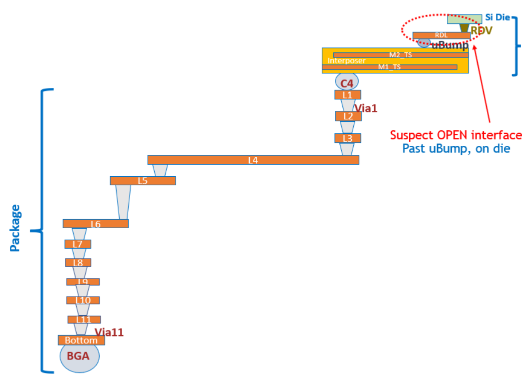

Figure 19. Cross-sectional view of traces and layers of failing signal. OPEN was isolated to the red-highlighted area.

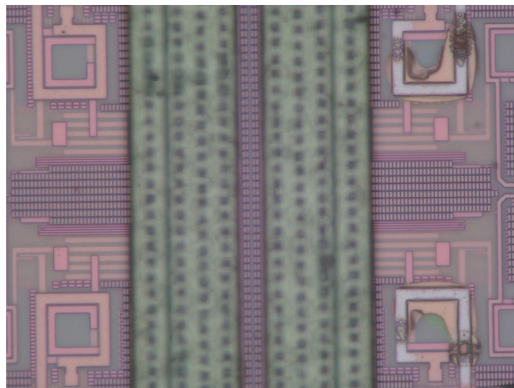

Figure 20. Optical micrograph showing EOS damage at the failing pins (on the right) after die removal. In the same field of view, good neighboring pins present (on the right) for reference.

EOTPR waveforms revealed that the high-impedance peak of the failing pin happened after the silicon interposer (Figure 18.) Consultation with the cross-sectional view of trace layers (in combination with the fact that this was a customer return failing in the field,) indicated that the fault was most likely on the silicon die (Figure 19), and highly possible due to an electrical overstress event. EOS damage was observed after the silicon die was removed (Figure 20.)

III. Conclusions

EOTPR has been proven to be an effective non-destructive fault isolation technique for chip-level FA, especially for IO failures. It was the technique of choice for signature analysis in Cases A and D, and it quickly identified the cause of failure in Cases B and C. For Cases E and F, EOTPR has helped us determine where to focus our analysis efforts: that we were able to follow up FI with the subsequent techniques that are most suitable for the defect location/type. We were also able to provide feedback to OSAT and Foundry partners in a timely manner. Our OSAT and Foundry partners can start their root-cause investigation while destructive PFA (which by its nature is labor-intensive and time-consuming,) is going in parallel.

EOTPR is now integrated in our FI workflow as the first non-destructive EFA technique to utilize in chip-level FA (Figure 21). While we continue to explore and extend its usefulness into silicon die, we are working to improve the throughput and workflow for volume FA so that we can enable EOTPR capability in OSAT/Foundry partners.

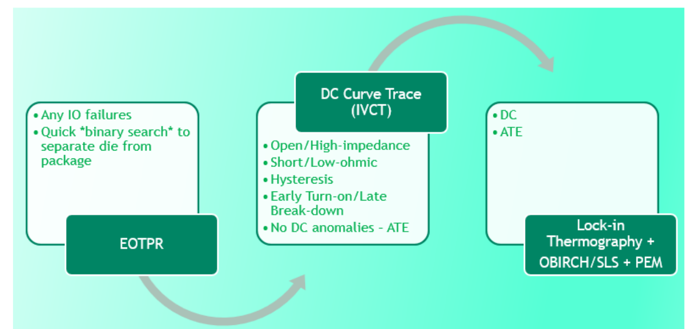

Figure 21. Non-destructive FI workflow for IO FA.

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