

High-Precision Pulse Reflectometry-Based Fault Localization Approach for Advanced Chip Package Failures

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Introduction

For decades, device scaling has been the primary driver of the performance boost in integrated circuit (IC) devices. However, this trend has slowed down in recent years due to physical limitations and technical challenges. To continue meeting the ever-increasing demand for high-performance computing, other innovations such as advanced transistor designs and packaging schemes have emerged. Advanced transistors, such as FinFETs and Gate-all-around FET (GAAFETs), have been developed to overcome the limitations of traditional planar transistors, offering higher performance and energy efficiency. Meanwhile, advanced packaging schemes, such as system-in-package (SiP), 2.5D, and 3D packaging (see Figure 1), offer higher integration densities, improved thermal management, and faster data transmission. These innovations are crucial in driving the development of high-performance computing, and they will play an essential role in meeting the growing demand for faster and more efficient computing [1].

High-performance computing chips have started adopting advanced packaging technologies that enable different dies to be heterogeneously integrated into a single chip package. Failure analysis plays a crucial role during the development and qualification of these advanced chip products. However, the increased complexity of these advanced chip packages makes conventional failure analysis methods less effective in localizing fault sites. Therefore, there is a growing need for innovative fault localization techniques and approaches that can accurately identify the root-cause defect within these complex packages [2].

The conventional time-domain reflectometry (TDR) method used for IC packaging fault isolation is an effective technique for measuring reflections of pulses that arise from the pulse's interaction with impedance changes in the packaging. This technique records these interactions as a function of their arrival time into a waveform, which can help locate faults. The increasing complexity of advanced packaging schemes, such as heterogeneous integration and 3D packaging, leads to more complex and heterogeneous interconnect structures, which can make it challenging to accurately identify and isolate faults using traditional TDR methods. As a result, an enhanced, pulse-signal based reflectometry, Electro-Optical Terahertz Pulse Reflectometry (EOTPR), has been developed and demonstrated to be a promising method for non-destructive fault isolation of advanced chip packages [3-6].

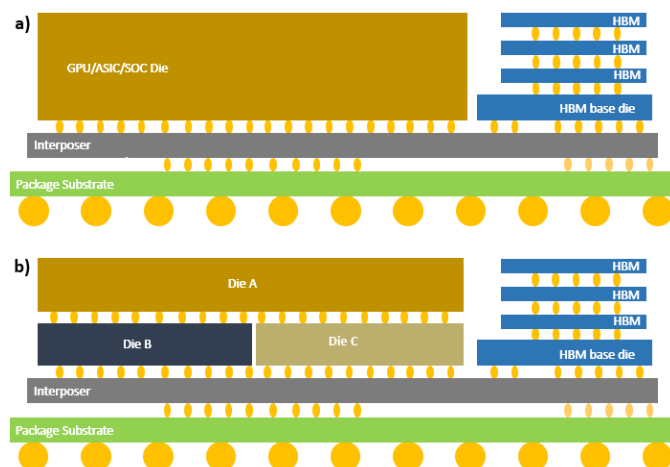


Figure 1: Schematics of advanced a) 2.5D and b) 3D packages

While pulse reflectometry is a powerful technique, it alone is insufficient for successful failure investigation. A comprehensive novel failure analysis approach, which incorporates pulse reflectometry along with other critical techniques such as simulation, reference sample preparations, X-ray tomography, and physical/material analysis methods, have been developed and will be discussed in this paper. By combining these different techniques, the fault site can be localized more efficiently and precisely. The workflow starts with high precision fault isolation, followed by non-destructive

and destructive analyses of the localized failure site to understand the failure mechanisms. This comprehensive approach has been proven to be a powerful solution for failure analysis for advanced chip packages.

Experimental

A FA approach of chip package continuity failure has been established and optimized as shown in figure 2.

This FA approach involves a series of steps to localize and characterize failures in complex chip packages. The first step in the FA workflow is bench verification, where the electrical failure mode is verified using IV curve tracing on the packaged chip. The next step is to collect EOTPR waveforms from both failed and reference known-good units.

Once the EOTPR waveforms are collected, the next step is to build a model of the failed IO trace in the chip package using the layout design information. An automated script has been created that extracts all the necessary information required for model generation from the layout design file, with the user simply specifying the chip product and the IO pin. The parameters in the generated model are then refined using the waveform collected from the known-good unit. Once the model is optimized, an open fault is injected into the model, and its location is refined to make the model-generated waveform match the waveform collected from the failed unit. By achieving a good fit between the simulated waveform and the measured waveform of the failed unit, the fault location within the trace can be extracted.

While this technique is efficient, it does not always provide high confidence localization of the fault site down to area that is sufficiently small for the next step physical analysis. To bridge this gap, an additional step can be conducted, by preparing the reference sample in ways to make the trace of interest terminated at multiple points around the EOTPR simulation predicted faulty location. It is important to prepare the reference sample with the trace of interest ending at the far-end of the range of predicted faulty location, collected EOTPR waveform from the reference sample, further prepare the sample to make the trace end at a point that is closer to the probe, collect another waveform. This practice can be repeated multiple times, if necessary, until the open peak in the waveform collected from the as-prepared reference sample shifts just passing that of the failure unit. By that time, the faulty location can be accurately pin-pointed to be between the last reference point and the reference point immediately before it.

After the fault site has been pin-pointed, subsequent physical analysis can be performed. X-ray tomography is a common step, it has the advantage of being a non-destructive analysis and provides 3D information of the structure surrounding the defect site. The 3D visualization of the surrounding structure often provides meaningful information during root-cause understanding. Knowing the exact fault site location, parallel lapping and cross-sectioning can be performed to enable high

resolution imaging of the failure site using optical microscopy or scanning-electron microscopy. Elemental analysis, such as electron dispersive spectroscopy(EDS), can also be performed on the prepared top-down or cross-sectional samples to gather information about the chemical composition at the fault location to help understand the potential process issues.

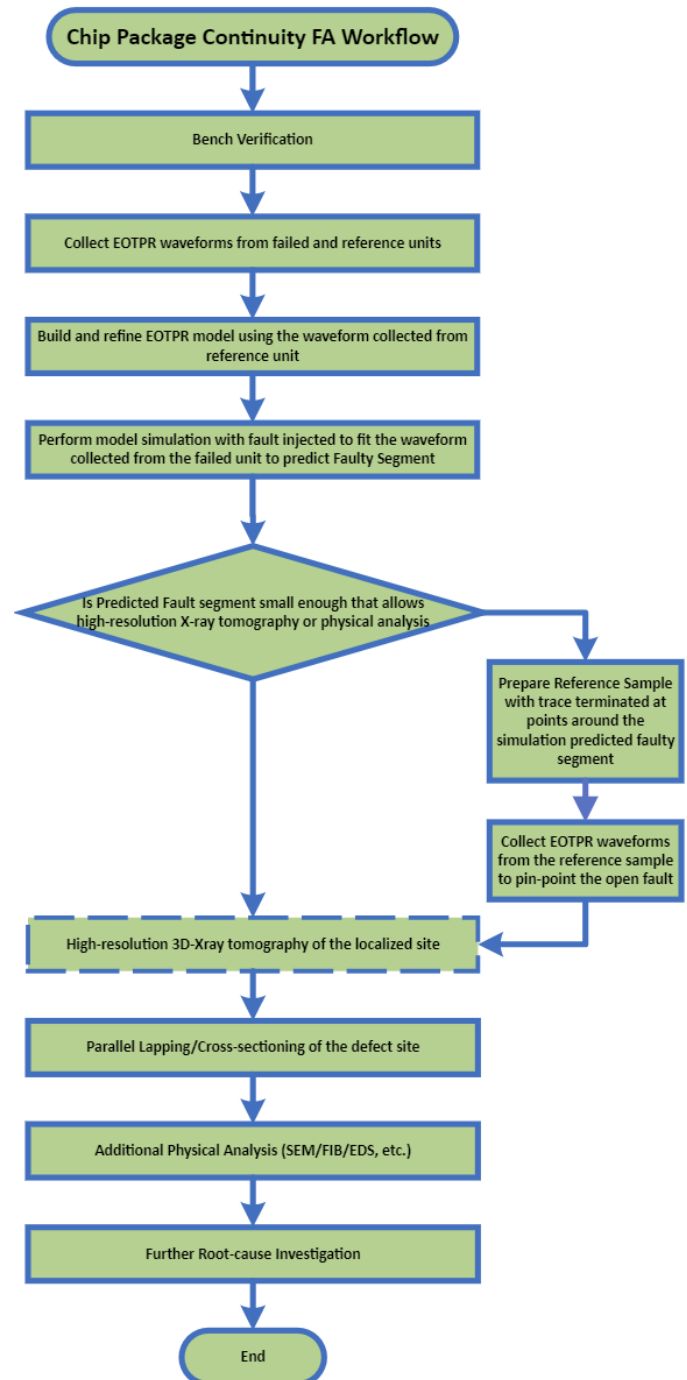


Figure 2. A workflow chart of chip package continuity FA approach

Results and Discussions

I. Pin-pointing defect in 2.5D package

The pulse reflectometry method using a combination of model simulation and reference points probing can be used to accurately and efficiently pin-point defects in advanced 2.5D and 3D chip packages.

A chip with 2.5D package was found to fail continuity open for a signal IO pin. After bench IV curve tracing confirmed open failure for the failed IO pin, EOTPR waveforms were collected on the failed IO pin from both the failed unit and a known-good reference unit. After that, EOTPR model was built using the layout construct information of the specific failure trace. The EOTPR model was refined using the waveform collected from the reference unit. As can be seen in Figure 3a, the model simulated waveform for the good unit (green, dotted line) has a good fitting with the measured waveform from the reference unit (green solid line). After that, an open fault was injected into the model, and the model was refined by changing the location of the open fault in the model to fit the waveform from the failed unit. Once a good fitting has been achieved, the location of the open fault can be extracted for the subsequent FA step. As can be seen in Figure 3a, the model fitted well with the waveform collected from failed unit, when the open fault is predicted to be within the circled segment of the pin trace in the schematics in Figure 3b.

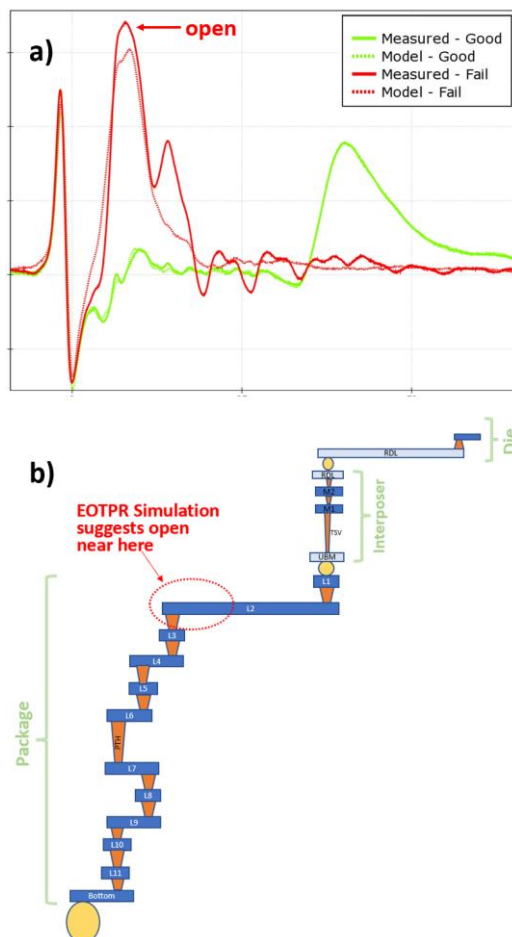


Figure 3: a) EOTPR simulated waveforms of the failed and reference units compared to the measured waveforms; b) The schematic of the failure trace with the segment predicted to contain open fault by EOTPR model simulation.

Since the suspect segment contains a via stack and the end of a long Level 2 trace line, it would be difficult to target the area through either X-ray tomography, top-down parallel lapping, or cross-sectioning. Therefore, terminal points were further created in the reference sample within the model-predicted faulty segment of the trace, by first mechanically remove the silicon dies, Si interposer, and layers above the Level 2 trace in the package substrate, and then cut on different locations in the level 2 trace of the IO pin, from locations farther away from the BGA, gradually moving towards the BGA direction as shown in the layout in Figure 4a. Multiple EOTPR waveforms were collected between the cuts and plotted together. As shown in Figure 4b, the open peak from the failed unit falls between the waveforms collected from the reference sample when it was cut between points 2 and 3. Therefore, the open defect in the failed unit was further pin-pointed to be at a location near the end of the M2 line within the trace at the exact location shown on the layout in Figure 4a.

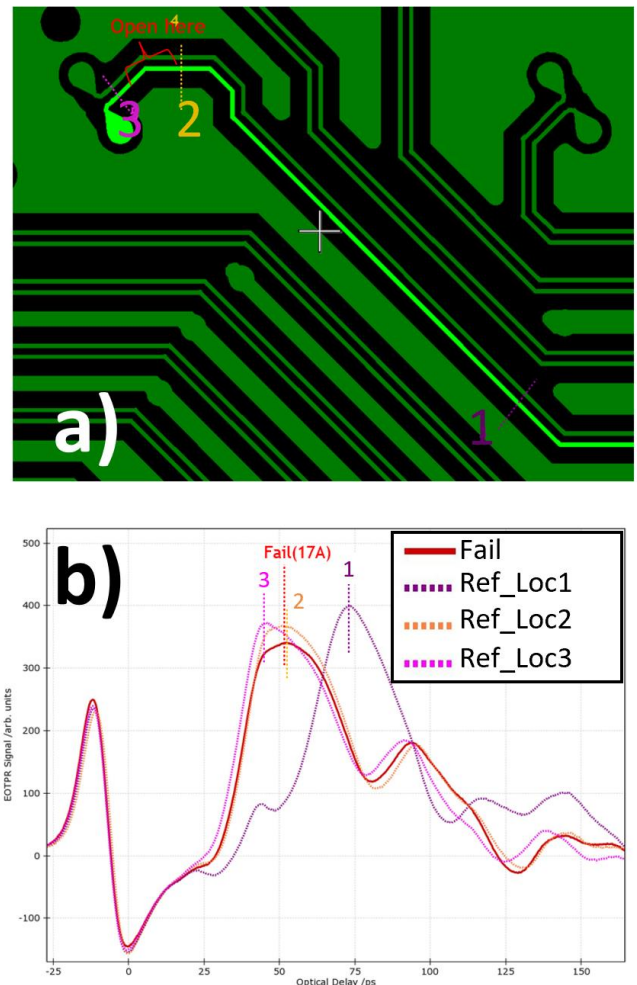


Figure 4: a) Layout schematics of the failure trace at L2 level, with the cut locations in reference sample highlighted; b) EOTPR waveforms collected from reference sample cut to terminate at these cut locations

With the open fault location pin-pointed, the failed unit was subsequently deprocessed, targeting to expose the predicted fault site and level. Subsequent optical imaging of the predicted location in Level 2 trace successfully found a defect responsible for open failure for the IO pin.

II. Synergistic application with 3D X-ray tomography

Depending on the failure modes, there are times 2D physical imaging methods through either parallel lapping or cross-sectional polishing do not provide sufficient information for the failure mechanisms understanding. This is when 3D X-ray tomography plays an instrumental role. In the example below, an open failure in a 2.5D packaged chip was localized with EOTPR simulation (Figure 5a) to be within a small segment at the lower levels of the package substrate, which consists of primarily vertical via stacks as shown in Figure 5b and its inset.

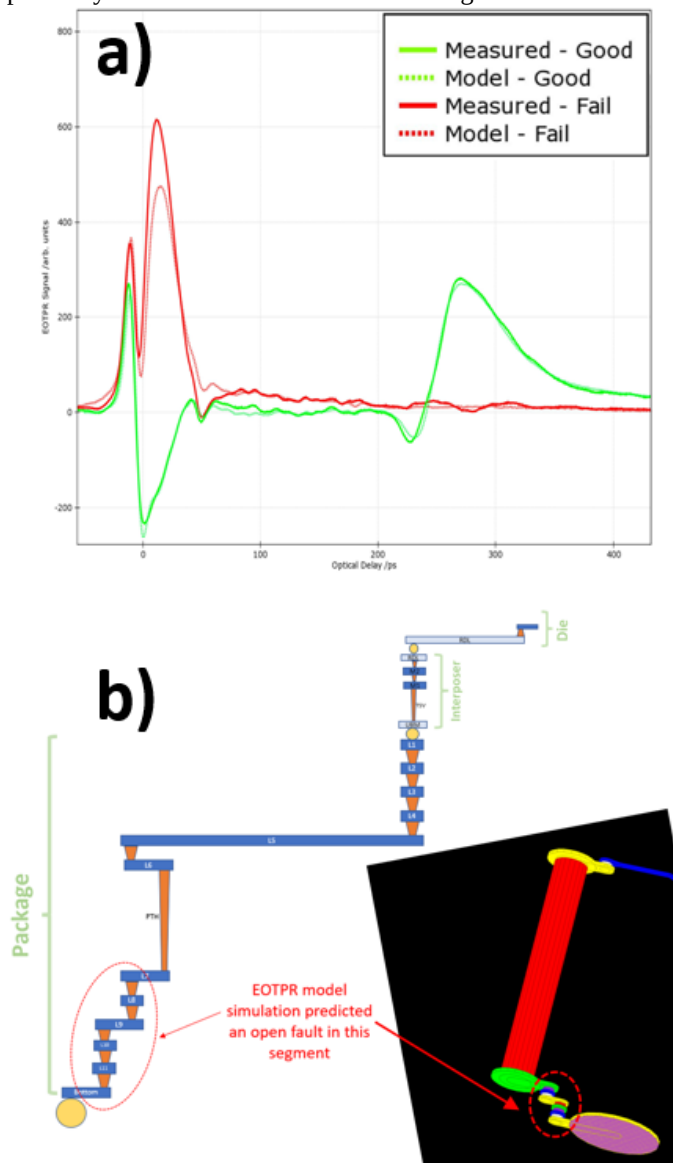


Figure 5: a) EOTPR simulation waveforms of the failed and reference units compared with their corresponding measurements waveforms; b) The schematics of the failure trace with the area predicted to contain open fault by EOTPR model simulation.

Since the via-stack segment is small enough for high-resolution 3D X-ray tomography to cover and clearly visualize. High resolution 3D X-ray tomography was subsequently performed, focusing on the suspect segment of the trace, which clearly showed a defect causing Level 9 trace open failure, within the segment predicted by EOTPR simulation.

III. Localizing defect in multiple-chip package

Similar method can also be used to localize faults in PCB assemblies, multiple-chip module (MCM) packages, chiplets or other heterogeneous integrated chip packages.

Figure 6 shows a schematic of a MCM package, in which the high speed link between Die A and Die B in the package were tested with fault.



Figure 6: schematic of a MCM package

The routing trace of the suspect high speed link in the package was first exposed and then cut in the middle to separate it into two segments, the left side goes into Die A, and the right side goes into Die B, as shown in Figure 7.

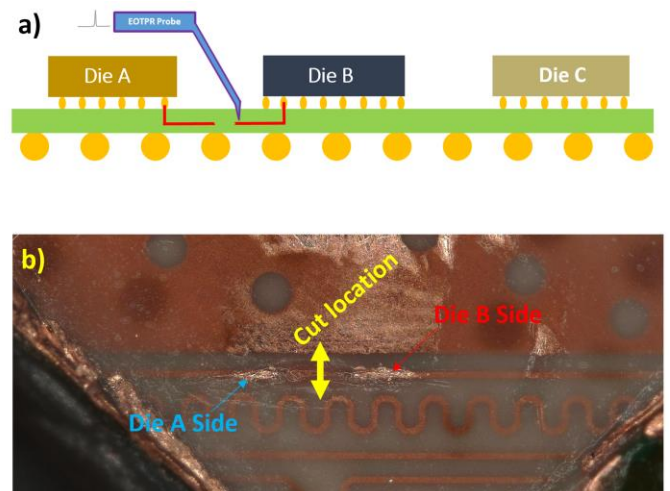


Figure 7: a) Schematic showing the trace in high speed link in the MCM package is cut in the middle; b) Optical image showing the trace in high speed link in the MCM package is exposed and cut in the middle

After that, IV curve tracing was performed on a micro-probing station on both sides of the trace. As shown in Figure 8, the connection to Die B showed a resistive open characteristics, which indicates that there is a resistive open fault on the half of the high speed link going into the Die B.

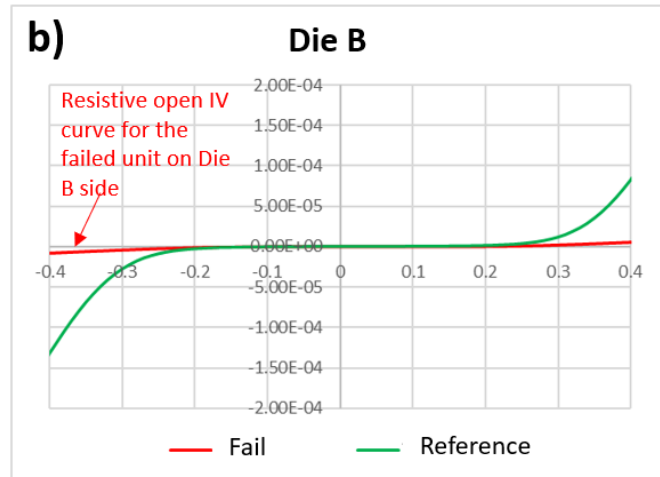
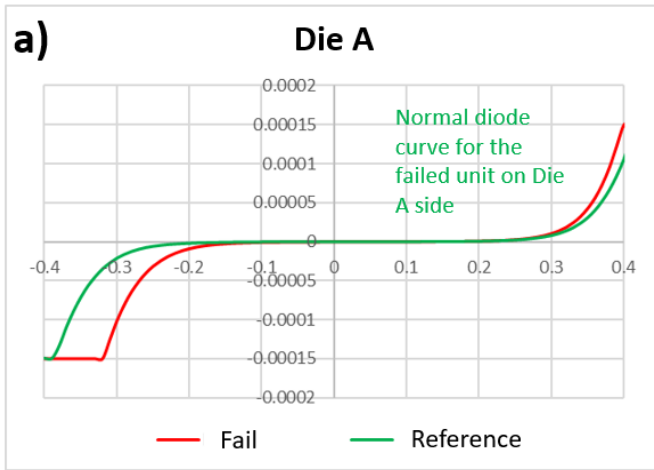


Figure 8: IV curve traces of the failure and reference units for a) segment going into Die A; b) segment going into Die B. Subsequently, EOTPR waveform was collected on the right side of the trace going into Die B from both the failed unit and a reference unit that was prepared the same way. EOTPR waveforms shown in Figure 9 has a high impedance peak for the failure unit.

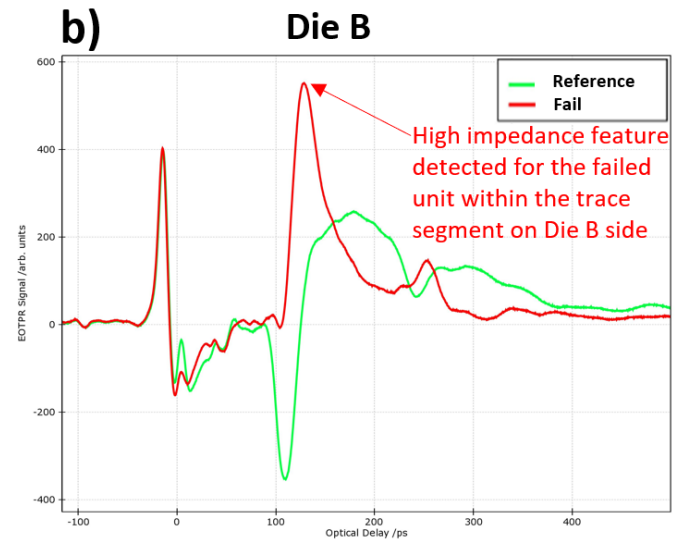
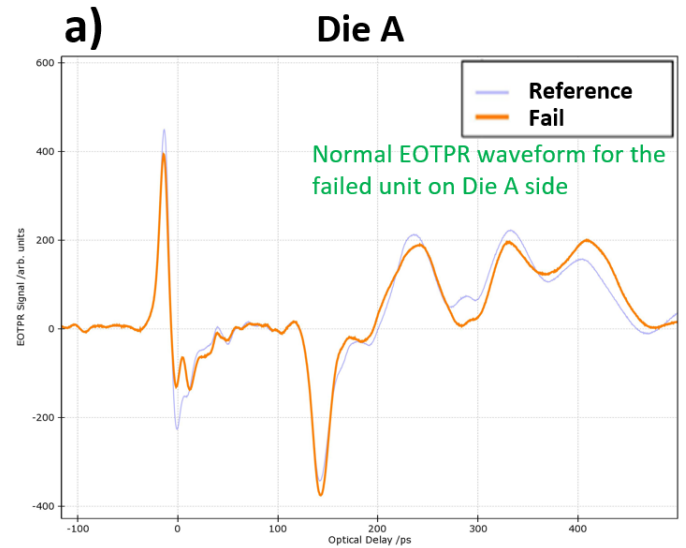


Figure 9: EOTPR waveforms collected from the failure and reference units for a) the segment going into Die A; b) the segment going into Die B

EOTPR model was then generated basing on the trace layout design for the half of the segment going into Die B. The waveform collected from the reference unit was used to refine the model to achieve a good fit. Subsequently, the model was used to simulate the waveform from the failed unit that predicted an open fault around the bump between Die B and the MCM package substrate.

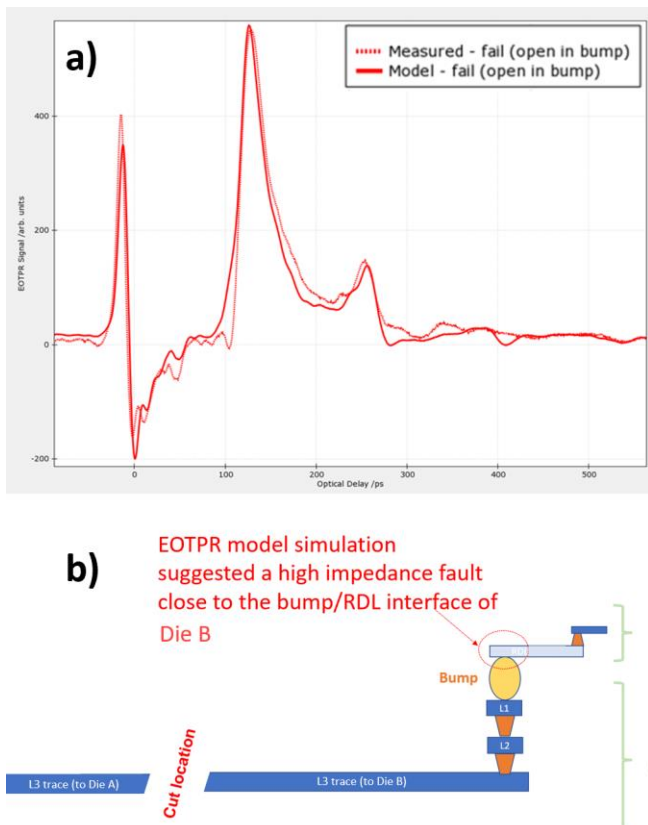


Figure 10: EOTPR simulation waveforms of the failed unit for the segment going into Die B; b) The schematics of the failure trace with the area predicted to contain open fault by EOTPR model simulation.

PFIB cross-sectional analysis was subsequently performed on the predicted failure bump interface and found an open defect there due to misprocess related issue.

Conclusions

During advanced chip package failure investigations, capturing and understanding root-causing failure modes could be challenging. An integrated methodology has been developed and discussed in this paper, which combines advanced pulse reflectometry with a suite of FA techniques. The workflow begins with high-precision EOTPR fault isolation with model simulation and reference point probing, followed by a comprehensive analysis involving both non-destructive and destructive techniques at the localized failure site to understand the root cause. This synergistic integration enhances FA efficiency and success rate, and has been proven to be a robust and potent solution for advanced package failure analysis.

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